In the Specification:

page 8, lines 4-8

FIG. 2A shows general implementation of present interconnect scheme, whereupon various endpoints 2(1), 2(2), ... , 2(N) are flexibly switched and/or routed through hardware block 10. Preferable, at least one improved endpoint is provided with serial to parallel converter circuit 6 or parallel to serial converter circuit 7, which each convert a multi-bitwidth (e.g., 32-bits) signal for sending to or receiving from one or more 1-bit wide signals generated by or transmitted by multiplexers in block 10.